

REMARKS

In the Official Action mailed on **01 November 2005**, the Examiner reviewed claims 1, 3-9, 11-17, and 19-27. Claims 1, 3, 4, 6-9, 11, 12, 14-17, 19, 20, and 22-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Li et al (USPN 6,208,183, hereinafter "Li") in view of any one of Self et al. (USPN 6,112,308 hereinafter "Self '308"), (USPN 6,009,532 hereinafter "Self '532") in view of Bar-Niv (USPN 5,631,591 hereinafter "Bar-Niv"), in view of Oman et al. (USPN 4,635,186 hereinafter "Oman"), in view of Eggebrecht et al. (USPN 4,495,594 hereinafter "Eggebrecht), in view of Lenk (USPN 6,538,516 hereinafter "Lenk"), in view of Chesavage (USPN 6,239,626 hereinafter "Chesavage '626"), in view of Locker et al. (USPN 6,577,174 hereinafter "Locker"), in view of Doblar et al. (USPN 6,516,422 hereinafter "Doblar"), in view of Smith et al. (USPN 6,925,135 hereinafter "Smith"), in view of Yabuki et al. (USPN 5,332,978 hereinafter "Yabuki"). and further in view of Chesavage (USPN 6,925,135 hereinafter "Chesavage '350"). Claims 5, 13, and 21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Li et al. any one of Self '308, Self '532 in view of Bar-Niv, Oman, Eggebrecht, and further in view of any one Lenk, Chesavage '626, Locker et al., Doblar et al., Smith et al., Yabuki et al., Chesavage '350, and further in view of Coleman et al (USPN 4,151,473, hereinafter "Coleman").

Rejections under 35 U.S.C. §103(a)

Independent claims 1, 9, and 17 were rejected as being unpatentable over Li in view of any one of Self '308, Self '532, Bar-Niv, Oman, and Eggebrecht and further in view of any one of Lenk, Chesavage '626, Locker, Doblar, Smith, Yabuki, and Chesavage '350.

Applicant respectfully points out that the **cited prior art references do not show any cross-coupled phase-lock loop (PLL) circuits**. In the prior art,

signals propagate in one direction between PLLs; there is no two-way feedback between PLLs.

Applicant notes that although PLLs may be coupled together in some existing systems to match phase relationships between the PLLs, no prior art references disclose cross-coupling two PLLs so that both operate at the speed of the slower PLL. Applicant respectfully points out that it is **not obvious** to cross-couple PLLs because in order to do so it is necessary to use something similar to the fairly complicated circuit in FIG. 2 (including the biasing circuit) that allows the PLLs to operate at the speed of the slower PLL.

Note that the present invention teaches a method to generate a maximum common frequency of two sources (see paragraphs [0023]-[0026] of the instant application). This is advantageous because it means that different chips can function together and communicate with each other at a maximum common frequency without a common clock, pre-synchronization, or any additional special preparation (see paragraphs [0037]-[0041] of the instant application). Moreover, the present invention facilitates multiple independently designed chips communicating with each other without special consideration from the chip designers during the design phase. **Applicant respectfully asks the Examiner to show two circuits on separate chips that are coupled together in such a manner that they operate at the speed of the slowest circuit.** Applicant points out that it is not obvious to do so, and that nothing in Li in view of any one of Self '308, Self '532, Bar-Niv, Oman, and Eggebrecht and further in view of any one of Lenk, Chesavage '626, Locker, Doblar, Smith, Yabuki, and Chesavage '350 teaches a method for generating a maximum common frequency to enable clocked chips to communicate with each other.

Hence, Applicant respectfully submits that independent claims 1, 9, and 17 as previously amended are in condition for allowance. Applicant also submits that claims 3-8 and 25, which depend upon claim 1, claims 11-16 and 26, which depend upon claim 9, and claims 19-24 and 27, which depend upon claim 17, are

for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

By



Edward J. Grundler

Registration No. 47,615

Date: 24 January 2006

Edward J. Grundler
PARK, VAUGHAN & FLEMING LLP
2820 Fifth Street
Davis, CA 95616-7759
Tel: (530) 759-1663
FAX: (530) 759-1665
Email: edward@parklegal.com